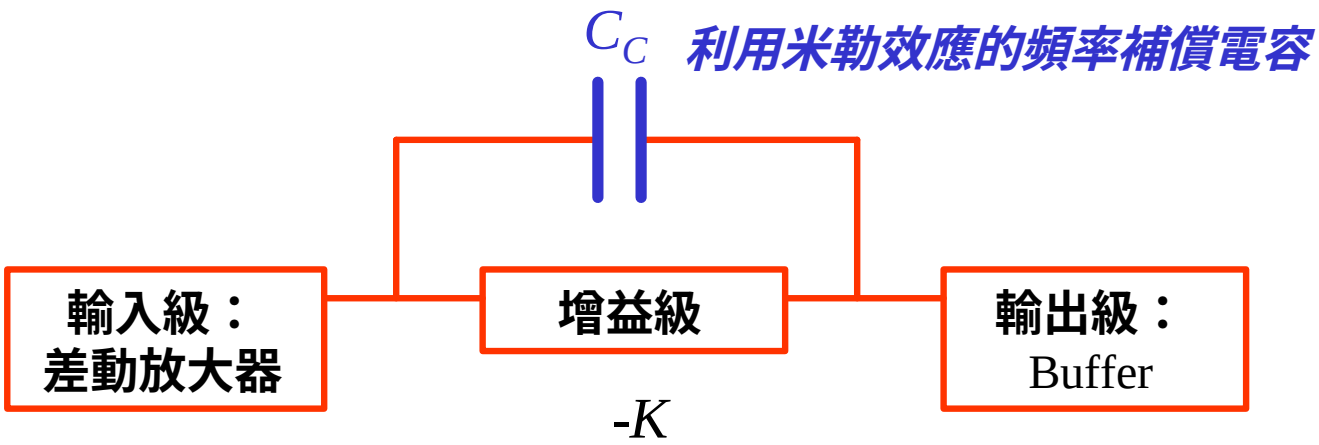
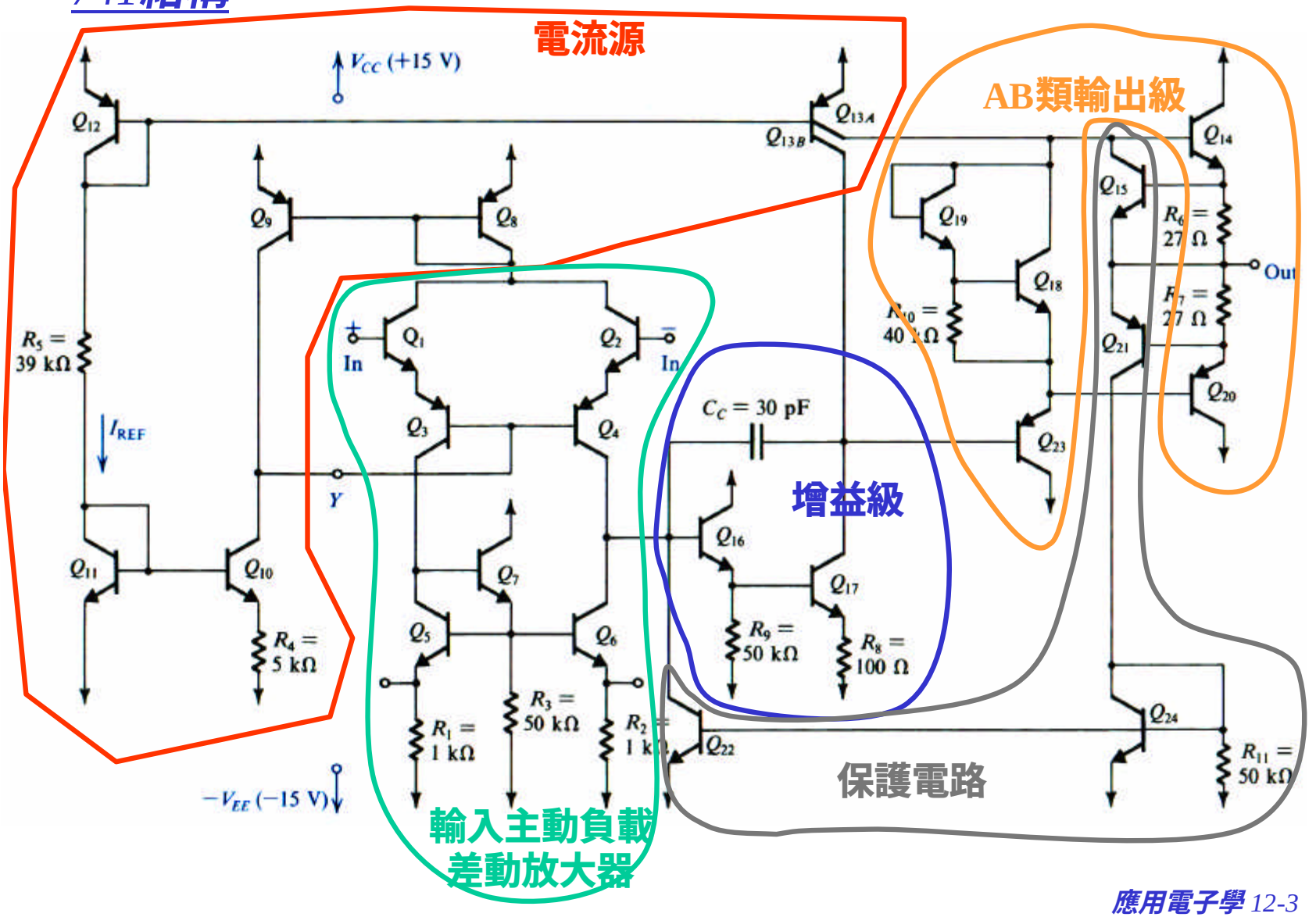
運算放大器內部結構

1. OP的結構
2. 741的結構
3. 741的直流分析
4. 741的小訊號分析
5. CMOS OP結構

*OP*一般結構



741結構


電流源
AB類輸出級
增益級
保護電路
輸入主動負載
差動放大器
V_{CC} (+15 V)
$-V_{EE}$ (−15 V)
Q_{12}
Q_{13A}
Q_{13B}
Q_9
Q_8
R_5 = 39 kΩ
I_{REF}
Q_{11}
Q_{10}
R_4 = 5 kΩ
Q_1
Q_2
In
In
Q_3
Q_4
Y
Q_7
Q_5
Q_6
R_1 = 1 kΩ
R_3 = 50 kΩ
R_2 = 1 kΩ
C_C = 30 pF
Q_{16}
Q_{17}
R_9 = 50 kΩ
R_8 = 100 Ω
Q_{22}
Q_{19}
Q_{18}
R_{10} = 40 kΩ
Q_{23}
Q_{14}
Q_{15}
R_6 = 27 Ω
Out
R_7 = 27 Ω
Q_{21}
Q_{20}
Q_{24}
R_{11} = 50 kΩ

741的直流分析

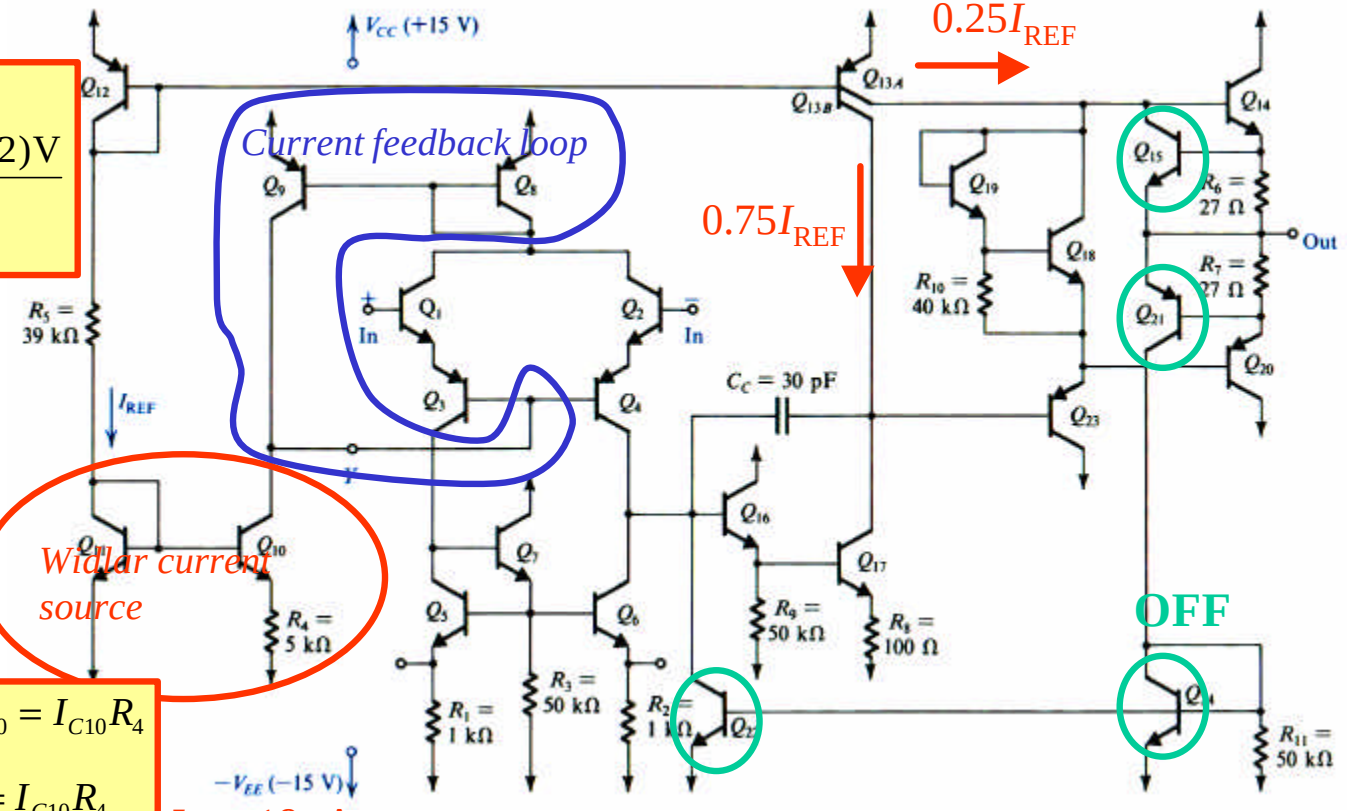
分析時用的元件參數：

npn: I_S=10^{-14}A, b=200, V_A=125V
pnp : I_S=10^{-14}A, b=50, V_A=50V

I_{SA}=0.25×10^{-14}A; I_{SB}=0.75×10^{-14}A

電流源分析

$$I_{REF} = \frac{(30-0.7\times2)\text{V}}{39\text{k}\Omega} = 0.73\text{mA}$$



$$V_{BE11} - V_{BE10} = I_{C10}R_4$$

$$V_T \ln\frac{I_{REF}}{I_{C10}} = I_{C10}R_4$$

I_{C10}=19μA

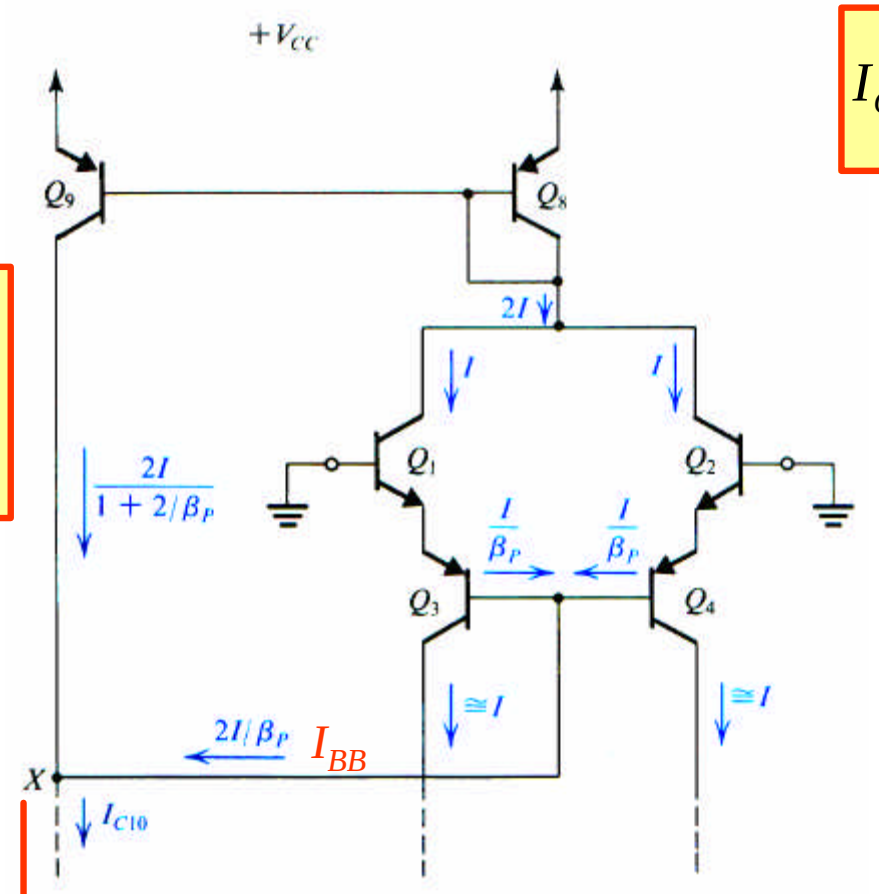
Current feedback loop of the first stage

$$I_{C9} = \frac{2I}{1 + 2/b_P}$$

$$I_{C1} = I_{C2} \approx I_{C3} = I_{C4} = 9.5mA$$

Input bias current

$$I_{B1} = I_{B2} = 9.5mA/200 = 47.5nA$$



I_{C10}=19μA

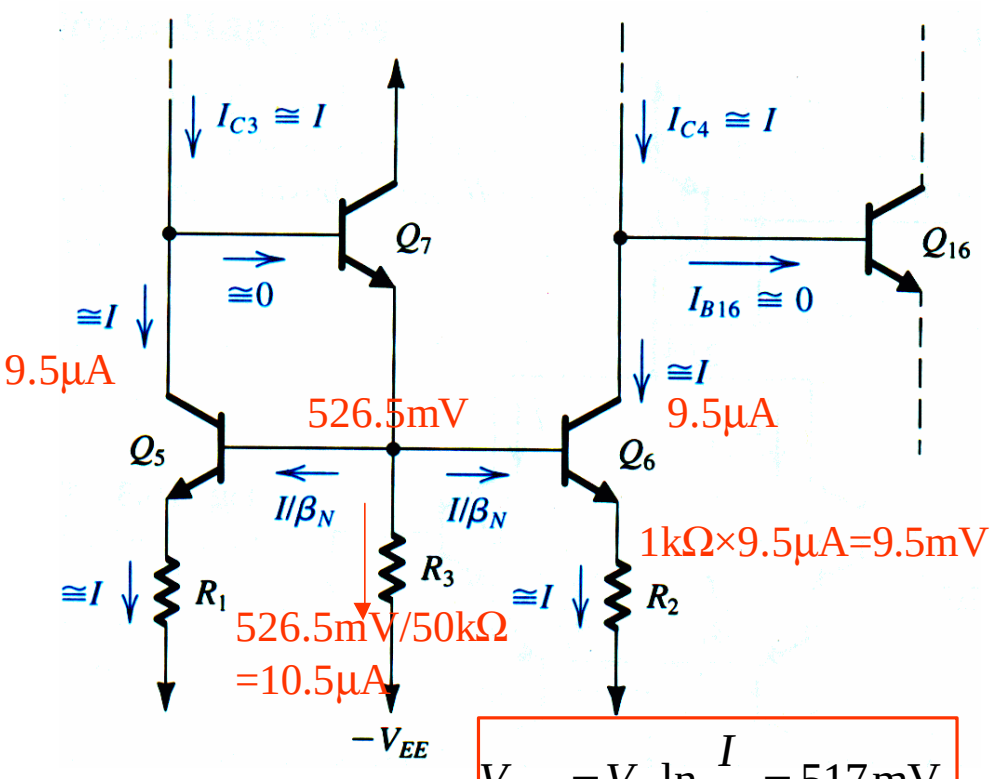
$I_{C1,2}$增加
→ I_{C8}增加
→ I_{C9}增加

但$I_{C9} + I_{BB} = I_{C10}$

→ I_{BB}減小
→ $I_{C1,2}$減小

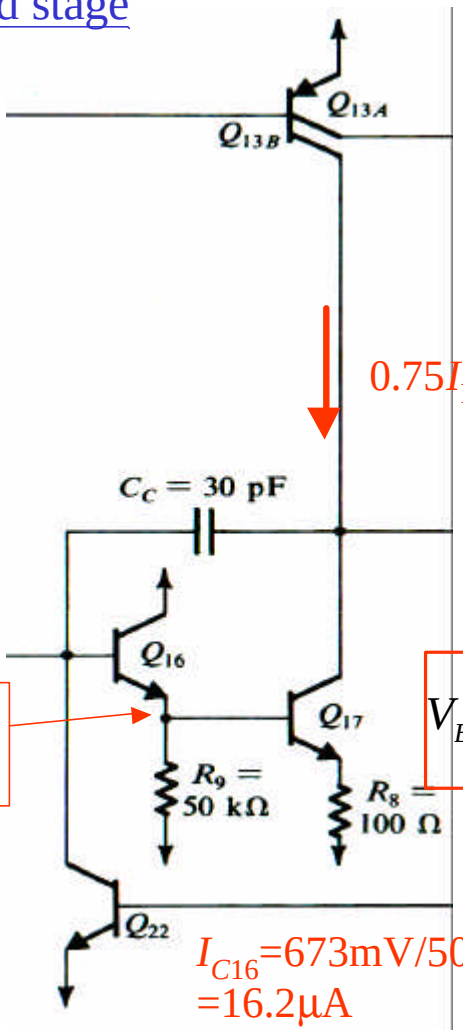
Load of the first stage amplifier

$R_{1,2}$用來增加負載阻抗，
R_3用來穩定Q_7的V_{BE}



$$V_{BE6} = V_T \ln \frac{I}{I_S} = 517\,\text{mV}$$

Bias current of the second stage



$0.75I_{REF}$=550μA

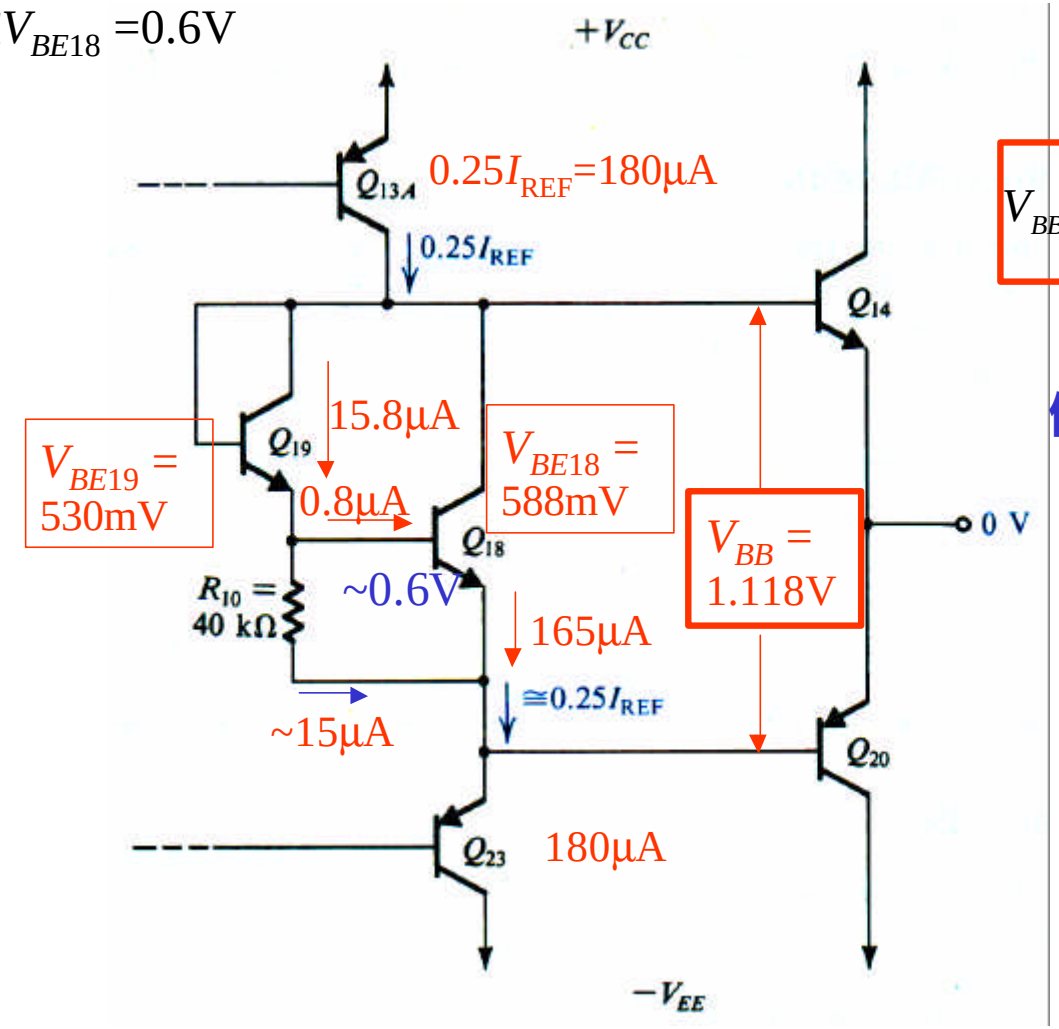
100Ω×550μA
+618mV=673mV

$$V_{BE17} = V_T \ln \frac{I_{C17}}{I_S} = 618\text{mV}$$

I_{C16}=673mV/50kΩ+550μA/200
=16.2μA

Output-state bias

要決定I_{E18}，先假設V_{BE18} =0.6V

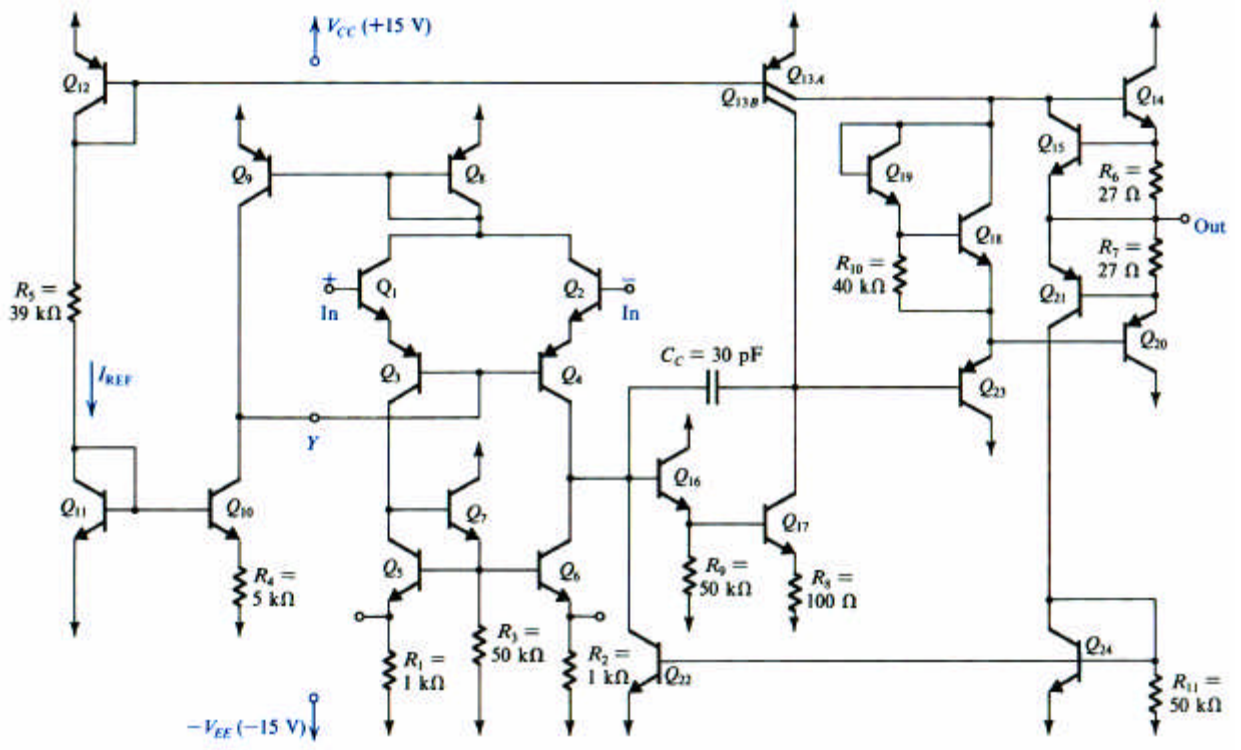


$$V_{BB} = V_T \ln\frac{I_{C14}}{I_{S14}} + V_T \ln\frac{I_{C20}}{I_{S20}}$$

假設I_{S14}= I_{S20}=3×10^{-14}A

I_{C14}= I_{C20}=154μA

結論

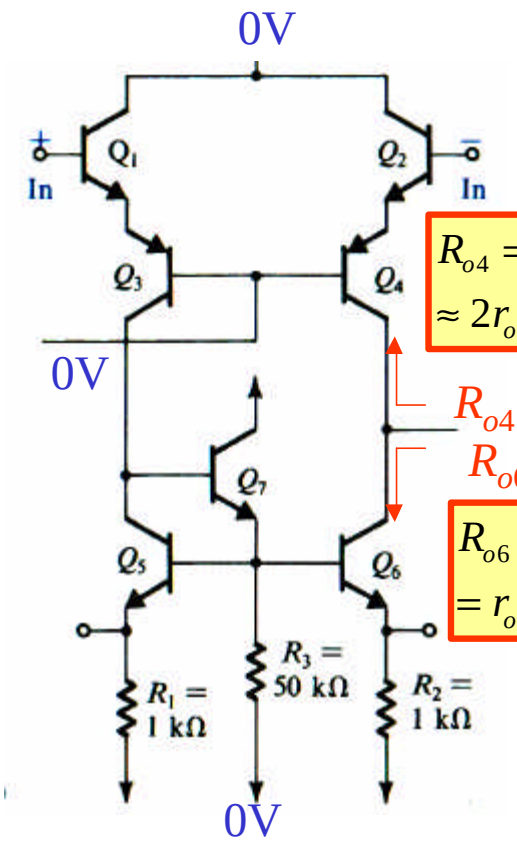


DC COLLECTOR CURRENTS OF THE 741 CIRCUIT (μA)

Q_1	9.5	Q_8	19	Q_{13B}	550	Q_{19}	15.8
Q_2	9.5	Q_9	19	Q_{14}	154	Q_{20}	154
Q_3	9.5	Q_{10}	19	Q_{15}	0	Q_{21}	0
Q_4	9.5	Q_{11}	730	Q_{16}	16.2	Q_{22}	0
Q_5	9.5	Q_{12}	730	Q_{17}	550	Q_{23}	180
Q_6	9.5	Q_{13A}	180	Q_{18}	165	Q_{24}	0
Q_7	10.5						

741的小訊號分析

Input stage: active-load differential amplifier

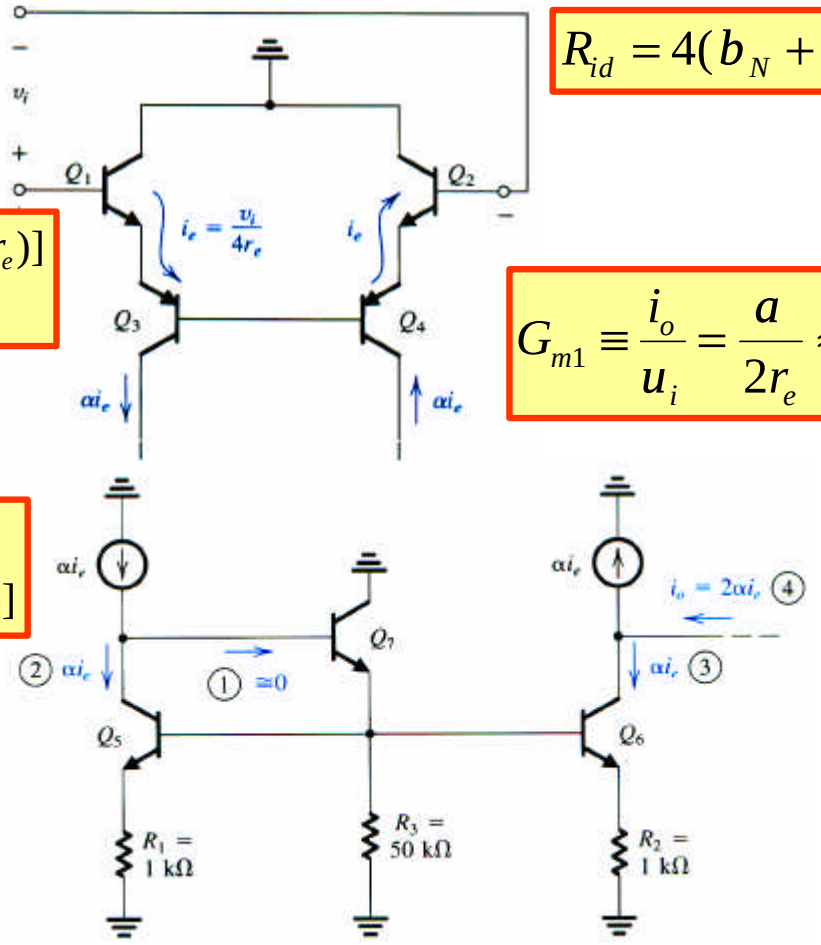


$$R_{o4} = r_o[1 + g_m(r_p \,//\, r_e)] \approx 2r_o$$

R_{o4}

R_{o6}

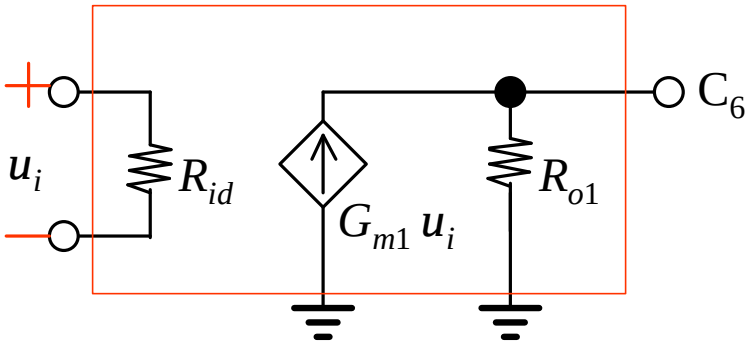
$$R_{o6} = r_o[1 + g_m(r_p \,//\, R_2)]$$



$$R_{id} = 4(b_N + 1)r_e$$

$$G_{m1} \equiv \frac{i_o}{u_i} = \frac{a}{2r_e} \approx \frac{g_m}{2}$$

Small signal model for the input stage of 741

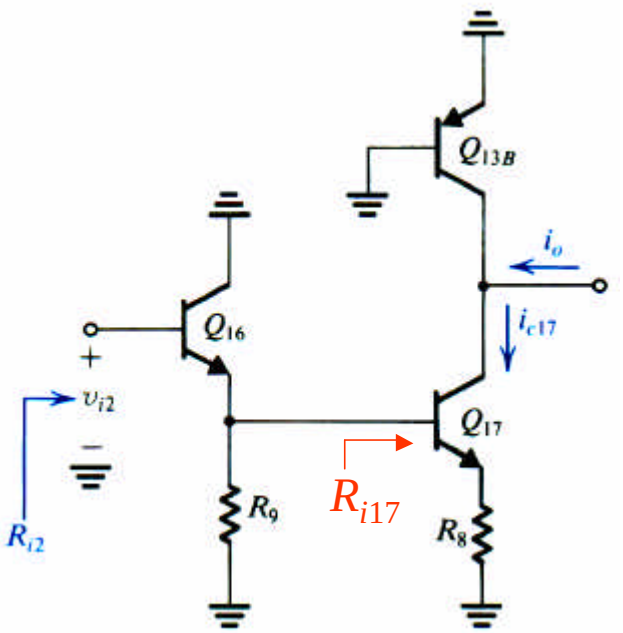


$$R_{id} = 4(b_N + 1)r_e$$
$$= 4 \times 201 \times \frac{25\text{mV}}{9.5\text{mA}}$$
$$= 2.1\text{M}\Omega$$

$$G_{m1} = \frac{a}{2r_e} \approx \frac{g_m}{2}$$
$$= \frac{1}{2 \times 2.63\text{k}\Omega}$$

$$R_{o1} = R_{o4} // R_{o6}$$
$$= 2r_o // r_o[1 + g_m(r_p // R_2)]$$
$$= (2 \times 5.26\text{M}\Omega) // (18.2\text{M}\Omega)$$
$$= 6.7\text{M}\Omega$$

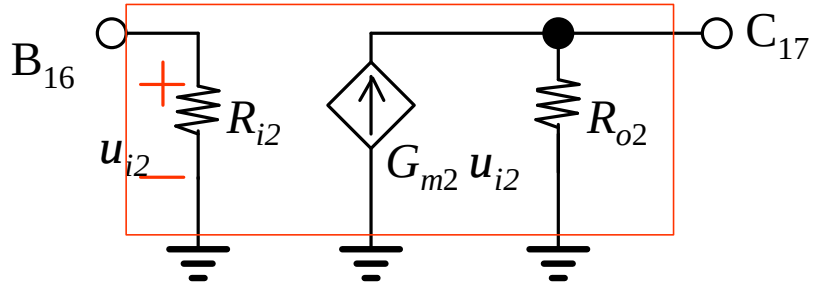
Small signal analysis for the 2nd stage---gain stage



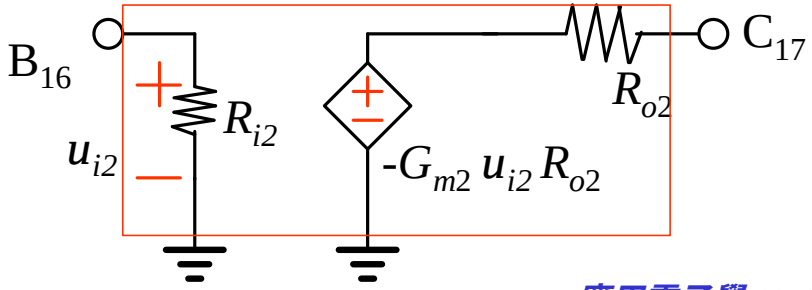
$$R_{o2} = R_{o13B} \,//\, R_{o17}$$
$$= r_{o13B} \,//\, r_{o17}\left\{1 + b_{17}\frac{R_8}{R_9 \,//\, [r_{e16} + R_{o1}/(b_{16}+1)] + r_{p17} + R_8}\right\}$$
$$= (90.9\text{k}\Omega)\,//\,(227.3\text{k}\Omega)\left\{1 + 200\frac{0.1}{50\,//\,[1.54 + 6700/(200+1)] + 9.1 + 0.1}\right\}$$
$$= (90.9\text{k}\Omega)\,//\,(380.1\text{k}\Omega)$$
$$= 73.4\text{k}\Omega$$

$$R_{oC} \approx \left[1 + b\frac{R_e}{R_B + r_p + R_e}\right] r_o$$

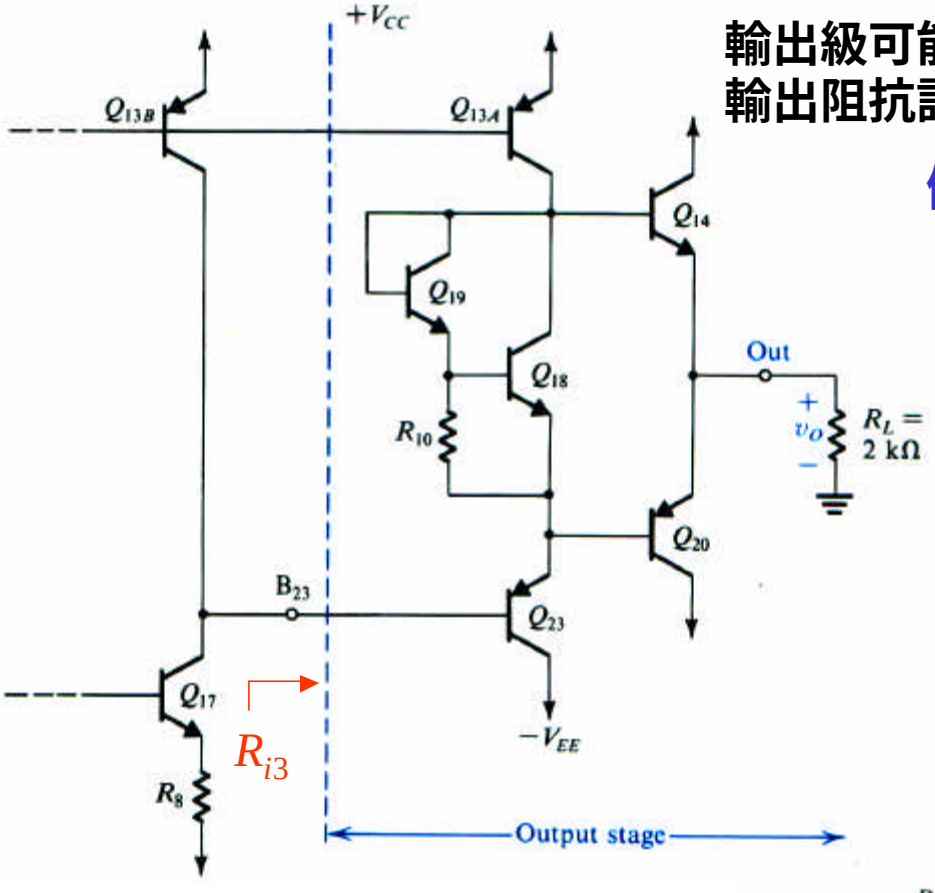
$$R_{i2} = (b_{16}+1)[r_{e16} + R_9 \,//\, (b_{17}+1)(r_{e17} + R_8)]$$
$$\approx 4\text{M}\Omega$$



$$i_{c17} \approx \frac{u_{b17}}{r_{e17} + R_8} = \frac{1}{r_{e17} + R_8} u_{i2} \frac{R_9 \,//\, R_{i17}}{(R_9 \,//\, R_{i17}) + r_{e16}}$$
$$R_{i17} = (b_{17}+1)(r_{e17} + R_8)$$
$$G_{m2} \equiv \frac{i_{c17}}{u_{i2}} \approx 6.5\text{mA/V}$$



Output stage of 741



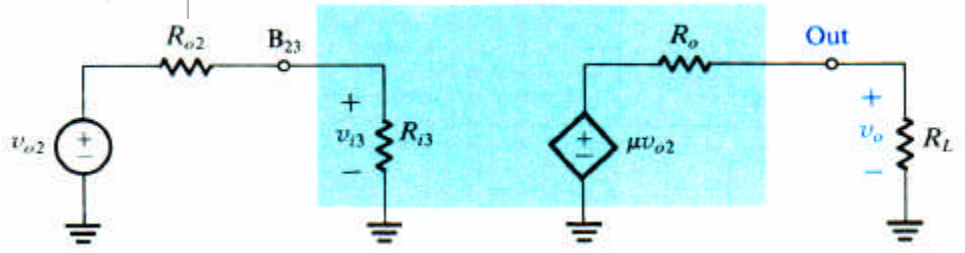
輸出級可能是Q_{14}或Q_{20} ON，會影響輸入和輸出阻抗計算。也同時和負載有關。

假設Q_{20} ON，電流為5mA。

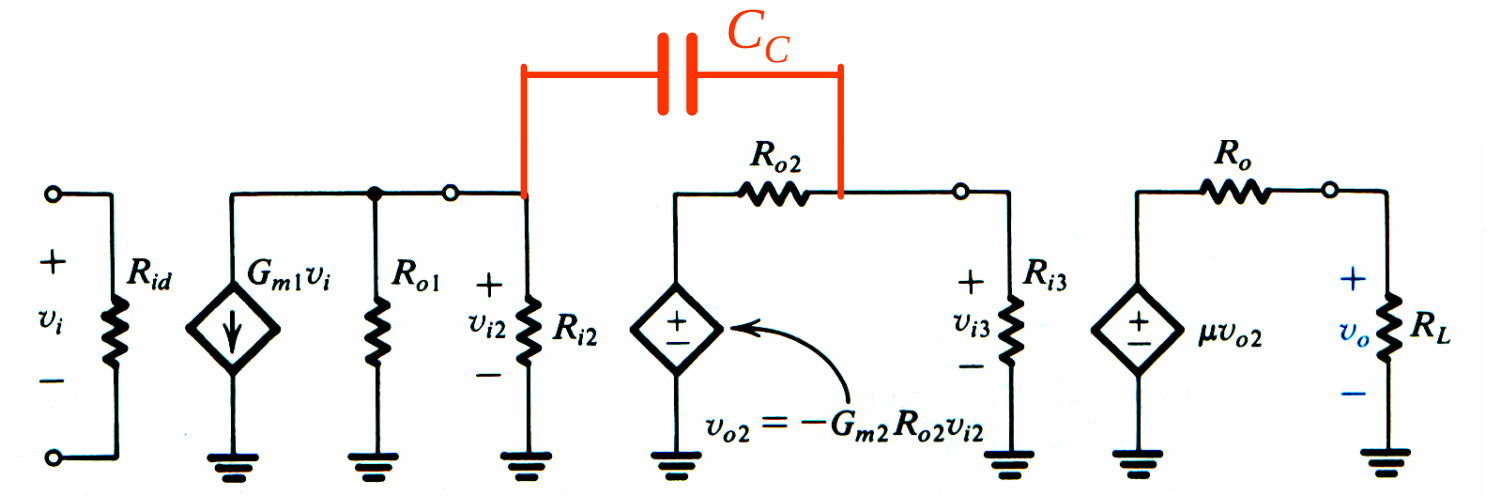
$$R_{i3} \approx b_{23}[r_{e23} + r_{o13A} // b_{20}(r_{e20} + R_L)]$$
$$= 50(280\text{k}\Omega // 50 \times 2\text{k}\Omega)$$
$$\approx 3.7\text{M}\Omega$$

$$R_o \approx r_{e20} + \frac{R_{o23}}{b_{20}} \approx r_{e20} + \frac{1}{b_{20}}\left(r_{e23} + \frac{R_{o2}}{b_{23}}\right)$$
$$= 5 + \frac{1}{50}\left(139 + \frac{73400}{50}\right) \quad \Omega$$
$$= 37\Omega$$

輸出級均為follower，
open-circuit gain**約為**1



Gain and frequency response of the 741



$$\frac{u_o}{u_i} = -G_{m1}(R_{o1} /\!/ R_{i2})(-G_{m2}R_{o2})\frac{R_{i3}}{R_{i3}+R_{o2}}m\frac{R_L}{R_L+R_o}$$

$$\approx -\frac{1}{5.26}(6700 /\!/ 4000)(-6.5\times 73.4)\frac{3700}{3700+73.4}\frac{2}{2+0.037}$$

$$= -476.2\times(-467.8)\times 0.98$$

$$= 218{,}720\text{V/V}$$

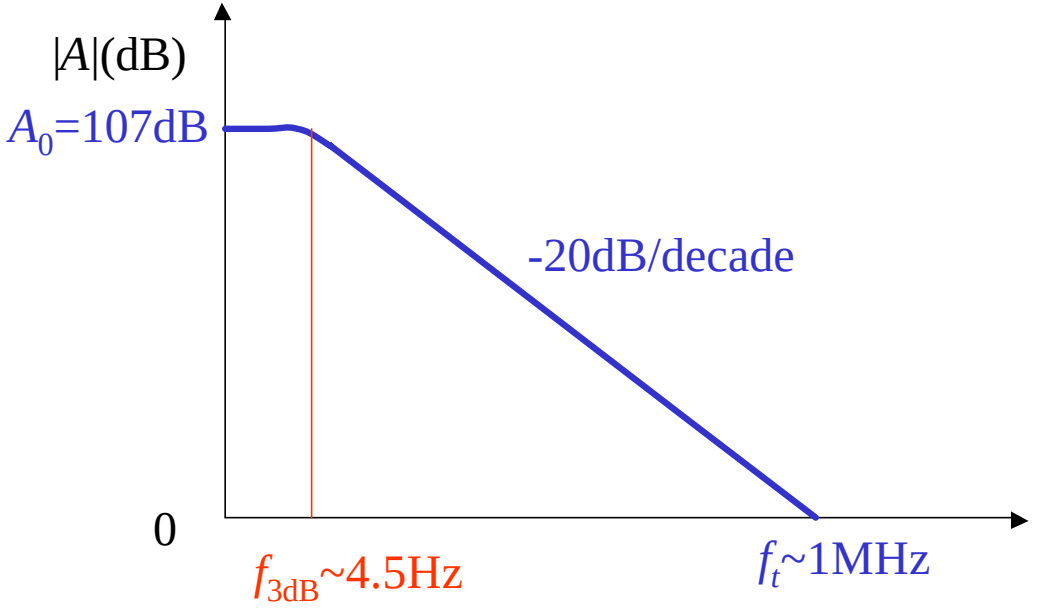
$$= 106.8\text{dB}$$

$$C_{eq} = C_C(1+|A_2|) = 30\text{pF} \times 469 = 14070\text{pF}$$

$$w_H = \frac{1}{C_{eq}(R_{o1} // R_{i2})} = \frac{1}{14070\text{pF}(6.7\text{M}\Omega // 4\text{M}\Omega)} = 28.4\text{rad/s}$$

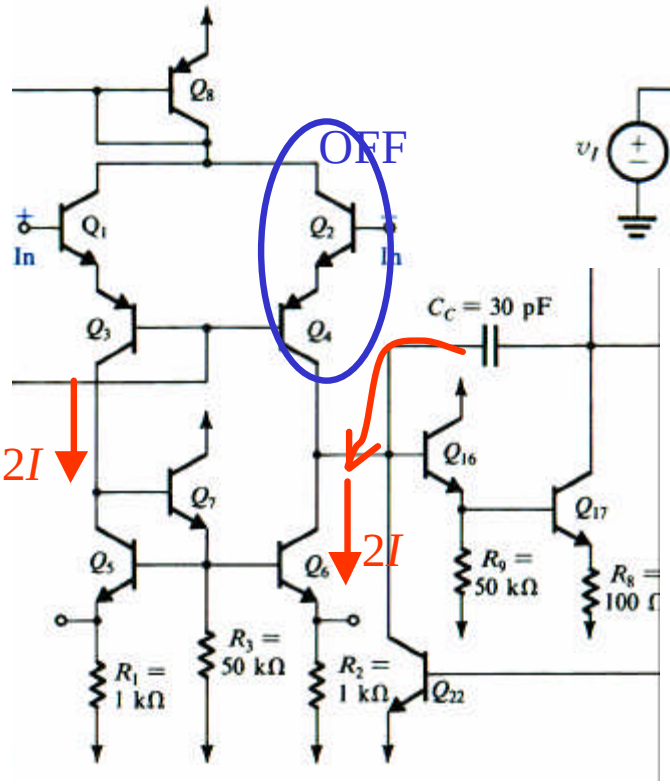
$$f_H = 4.5\text{Hz}$$

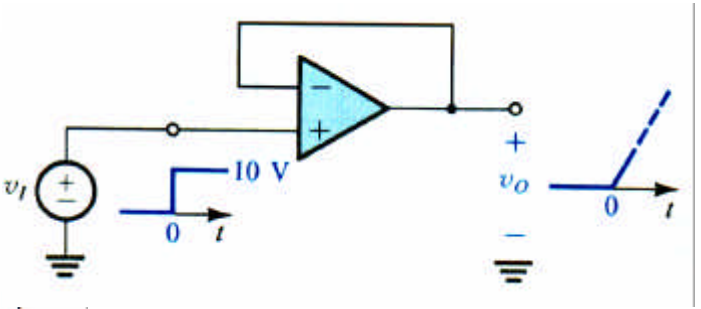
$$f_T = A_0 f_H = 984\text{kHz} \approx 1\text{MHz}$$



Slew rate (SR)

輸出電壓最大的變化速率(V/s)，**會限制**full-power bandwidth





測試電路

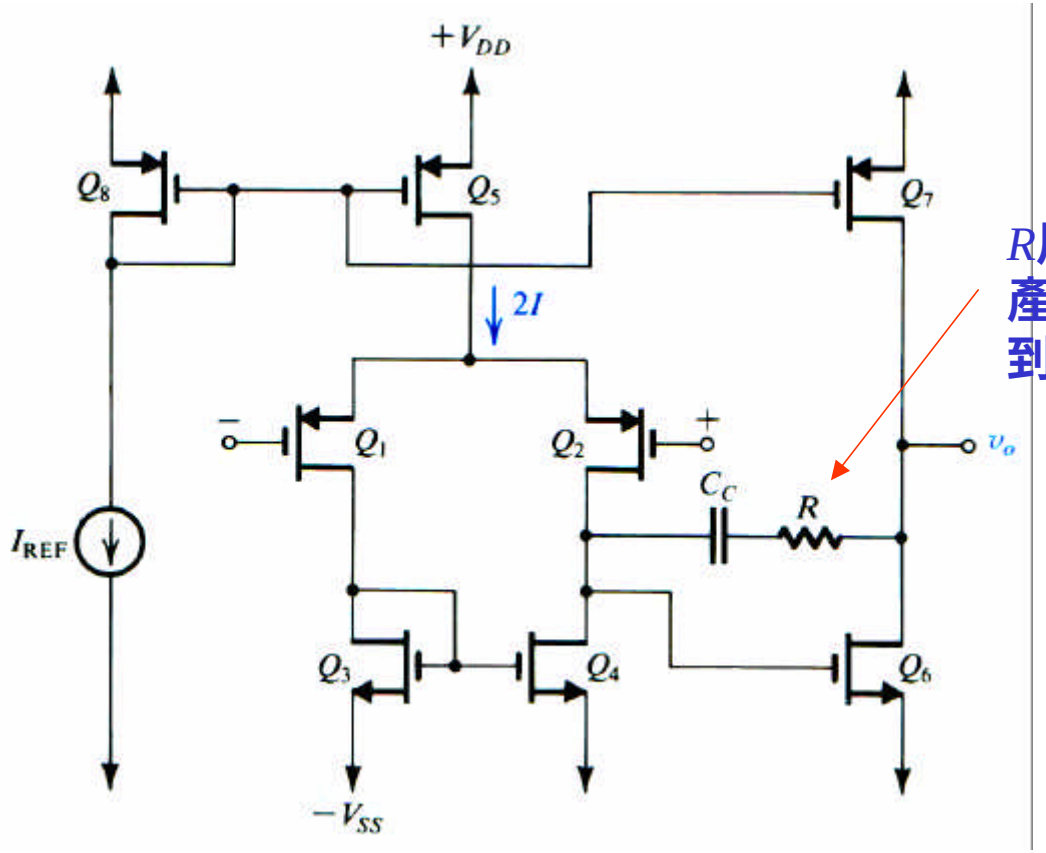
$$u_O(t) = \frac{2I}{C_C}t$$

$$\text{SR} = \frac{2I}{C_C}$$

$$= \frac{2 \times 9.5\mu\text{A}}{30\text{pF}} = 0.63\text{V}/ms$$

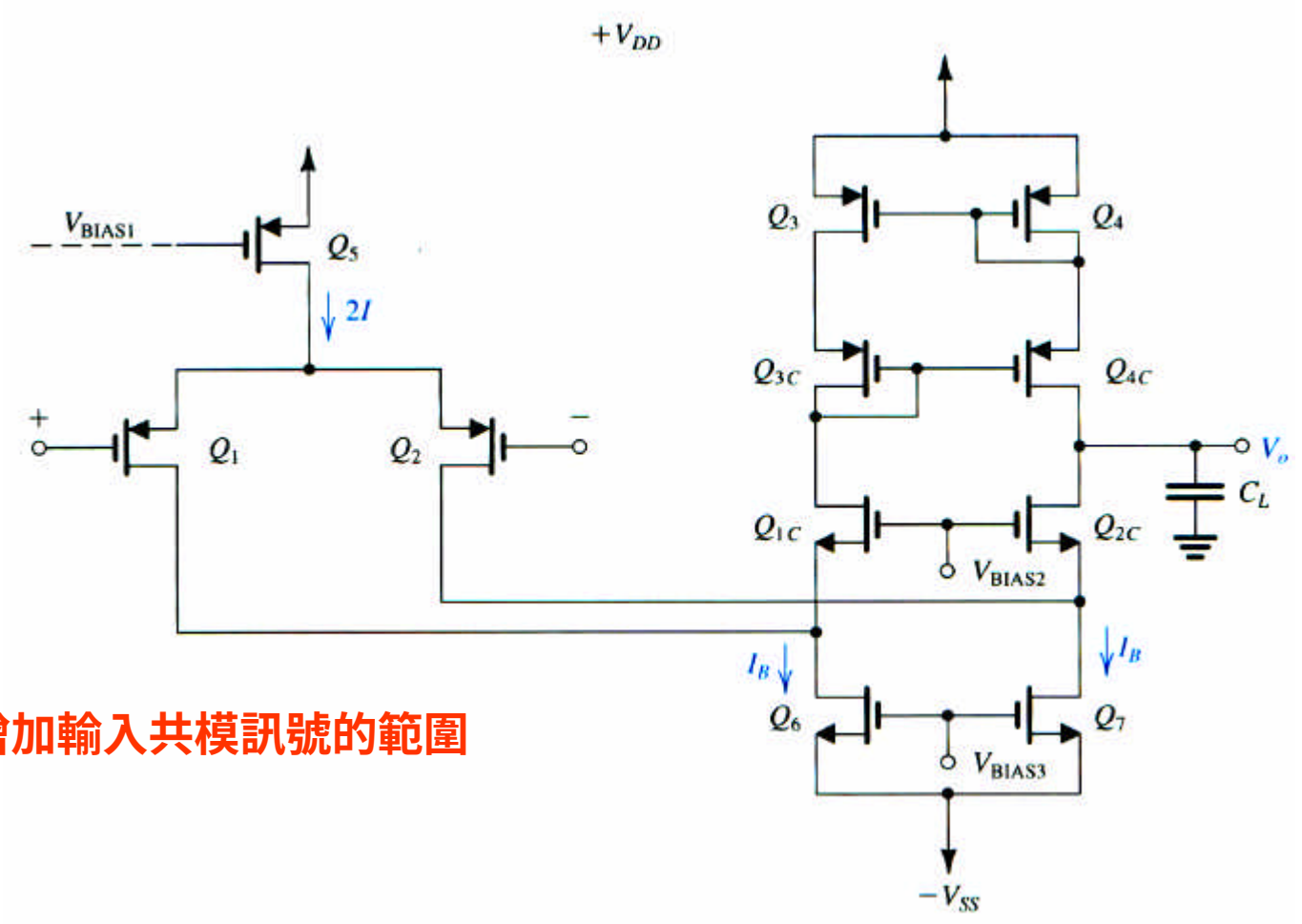
CMOS OP結構

基本型



R用來將其所產生的zero移到更高頻

Folded-cascode CMOS OP amp



增加輸入共模訊號的範圍