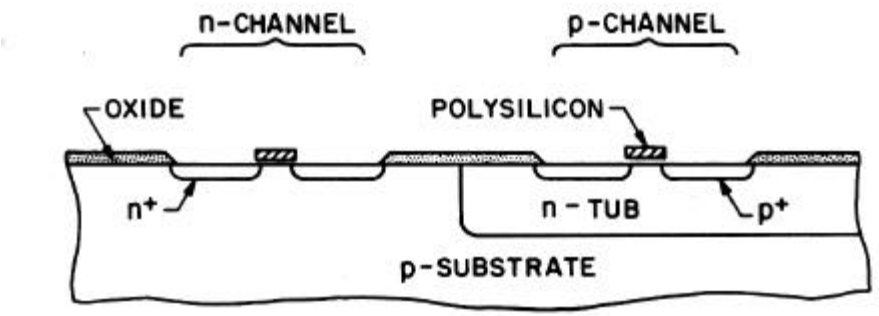
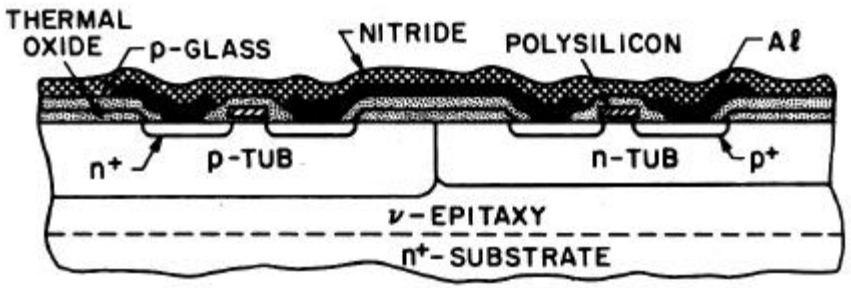
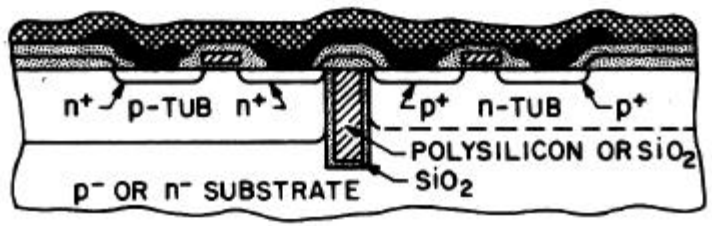
CMOS數位邏輯

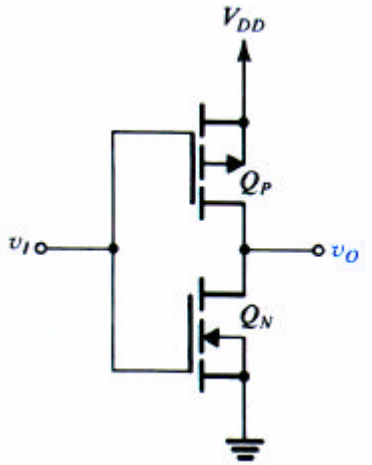
Complementary MOS or CMOS technology

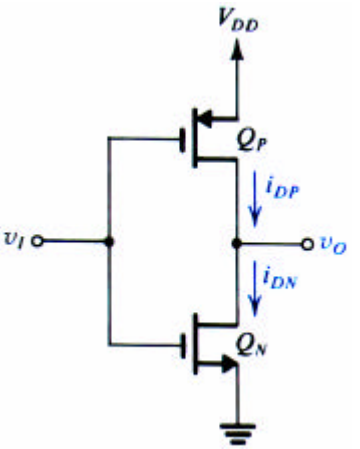


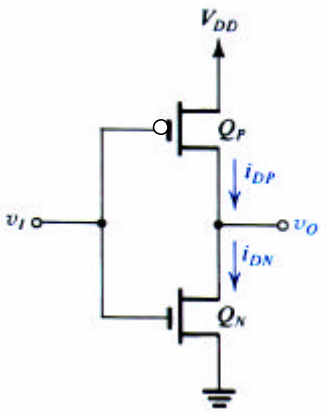




反相器（反閘）

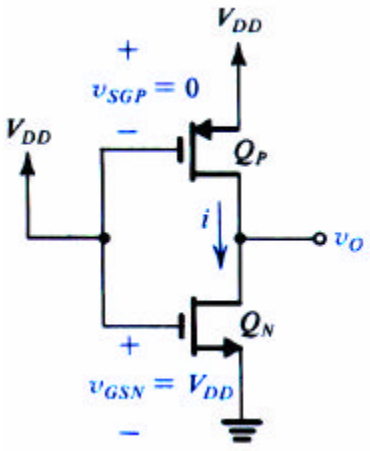


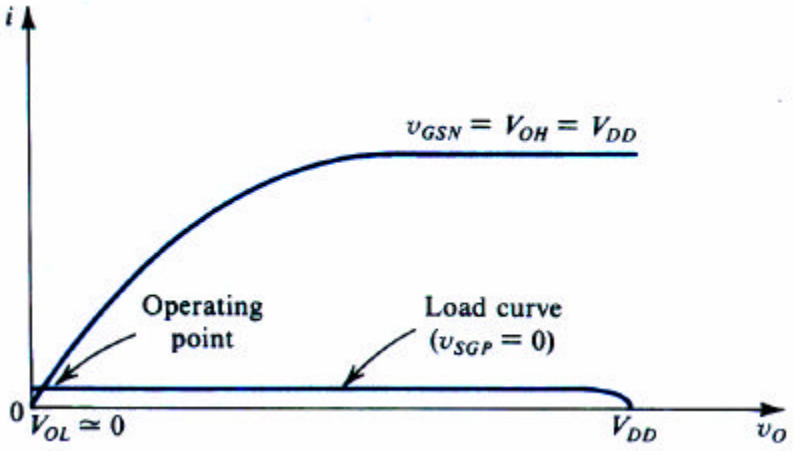


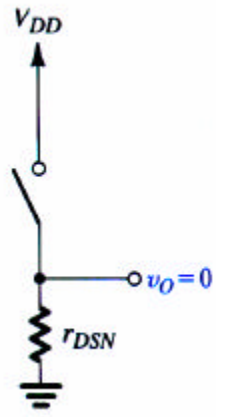


反相器的操作

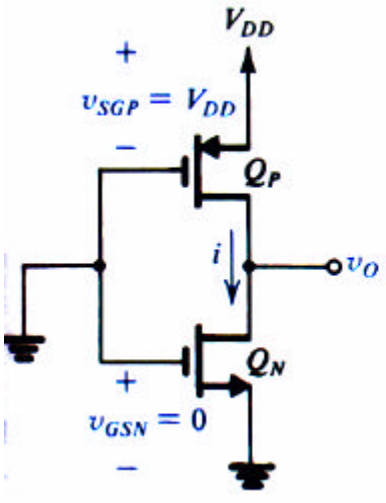
當輸入為高電位(Hi, 1)

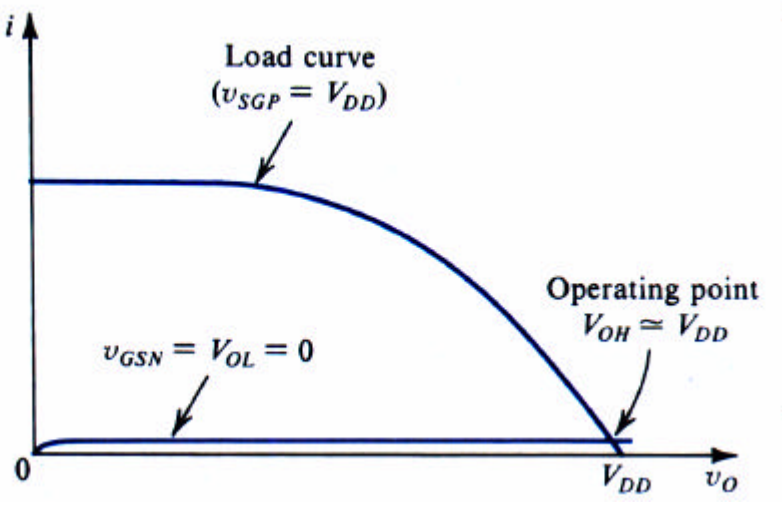


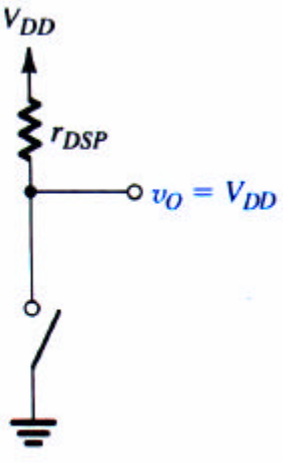




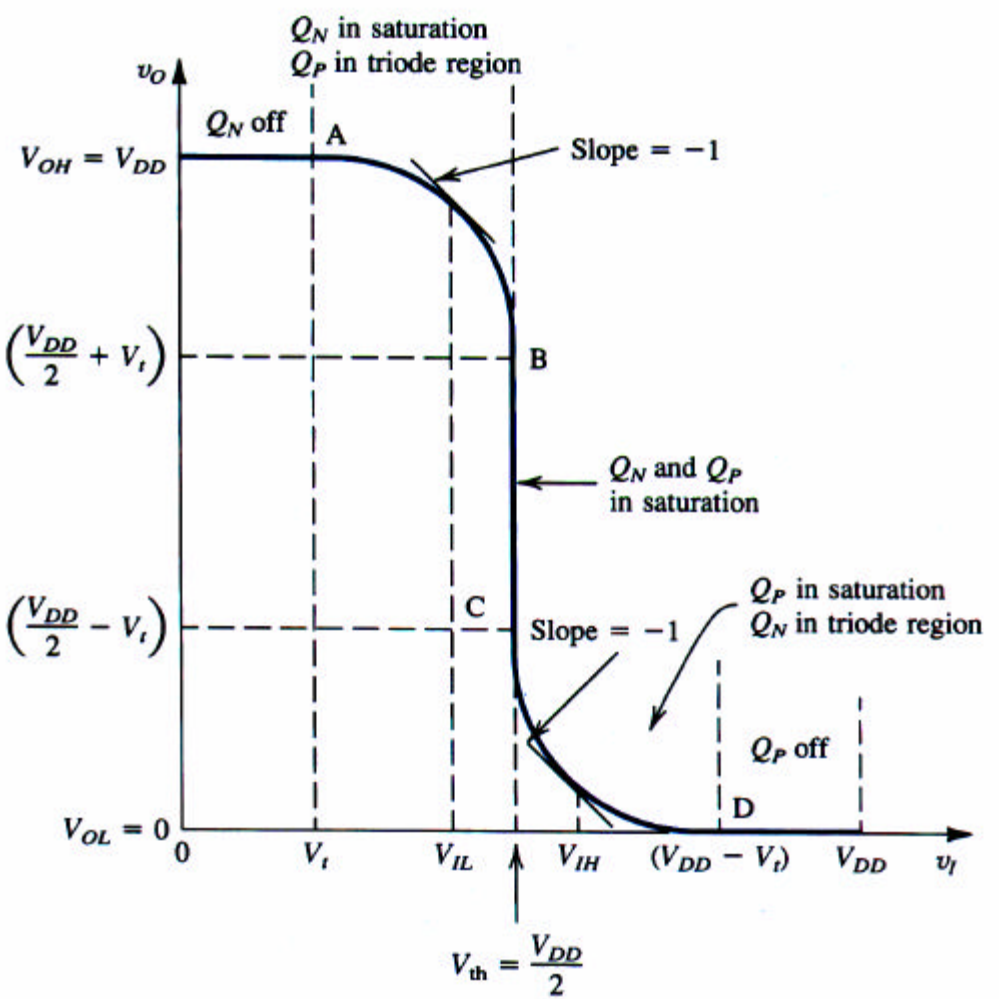
當輸入為低電位(Lo, 0)







反相器的轉換特性

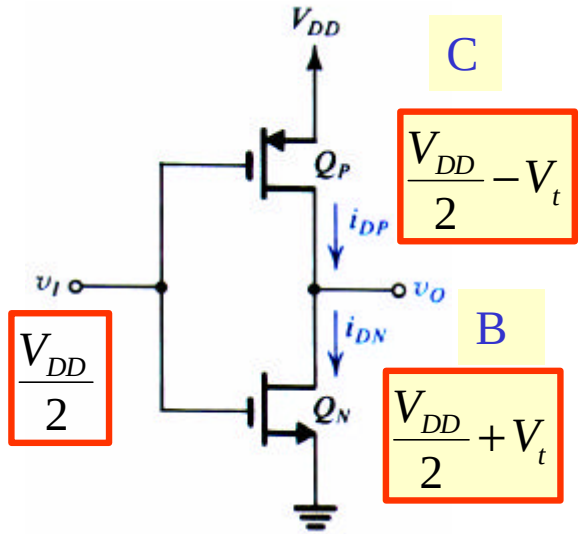


選擇元件參數使得：

$$k_n'\left(\frac{W}{L}\right)_n = k_p'\left(\frac{W}{L}\right)_p \quad \text{or}$$

$$\frac{W_p}{W_n} = \frac{m_n}{m_p} \quad \text{and}$$

$$|V_{tn}| = |V_{tp}| = V_t$$



應用電子學 8-45 中興物理 孫允武

計算V_{IL}和V_{IH}

定義為轉換曲線上斜率為-1對應的輸入電壓。

考慮CD間曲線，此時之Q_N在triode區， Q_P在sat.區，符合

$$(u_I - V_t - \frac{1}{2}u_O)u_O = \frac{1}{2}(V_{DD} - u_I - V_t)^2$$

兩邊對u_I微分

$$(u_I - V_t)\frac{du_O}{du_I} + u_O - u_O\frac{du_O}{du_I} = -(V_{DD} - u_I - V_t)$$

令

$$u_I = V_{IH} \qquad \frac{du_O}{du_I} = -1$$

解得

$$u_O = V_{IH} - \frac{V_{DD}}{2} \qquad V_{IH} = \frac{1}{8}(5V_{DD} - 2V_t)$$

同理可推導得

$$V_{IL} = \frac{1}{8}(3V_{DD} + 2V_t)$$

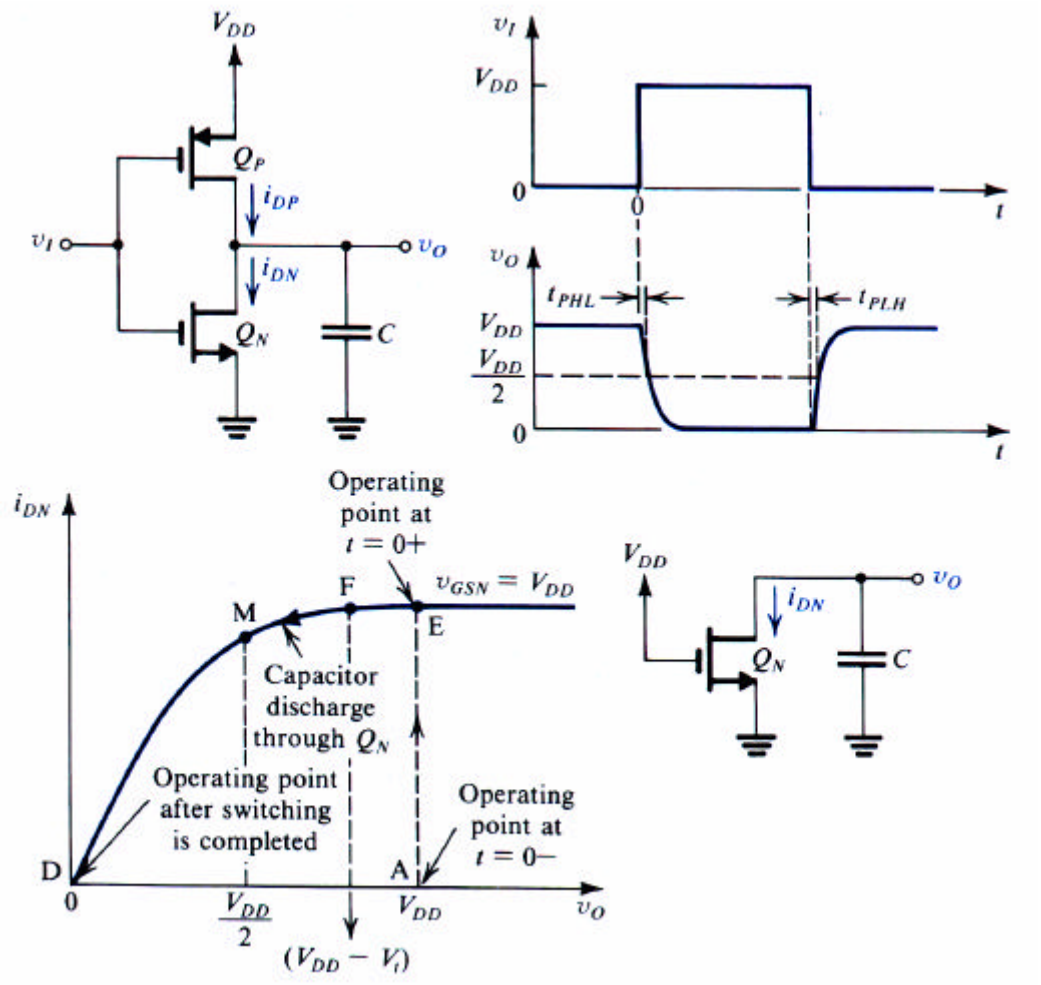
計算noise margin

$$NM_H = V_{OH} - V_{IH} = V_{DD} - \frac{1}{8}(5V_{DD} - 2V_t) = \frac{1}{8}(3V_{DD} + 2V_t)$$

$$NM_L = V_{IL} - V_{OL} = \frac{1}{8}(3V_{DD} + 2V_t) - 0 = \frac{1}{8}(3V_{DD} + 2V_t)$$

動態特性與功率耗散

Propagation delay 傳遞延遲



假設$V_t \sim 0.2V_{DD}$

$$t_{PHL} = \frac{1.6C}{k_n'(W/L)_n V_{DD}}$$

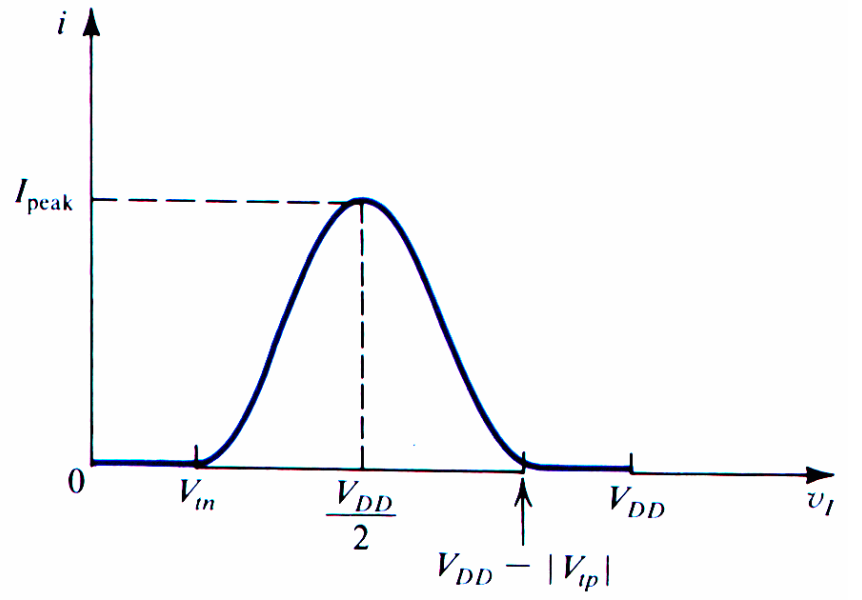
$$t_{PLH} = \frac{1.6C}{k_p'(W/L)_p V_{DD}}$$

Delay-Power Product 延遲功率乘積

CMOS反相器(或其他邏輯閘)只有在狀態轉換時，才有功率損耗。每週期損耗為CV_{DD}^2，Q_P和Q_N各半。

若開關的頻率為f，則功率耗散為

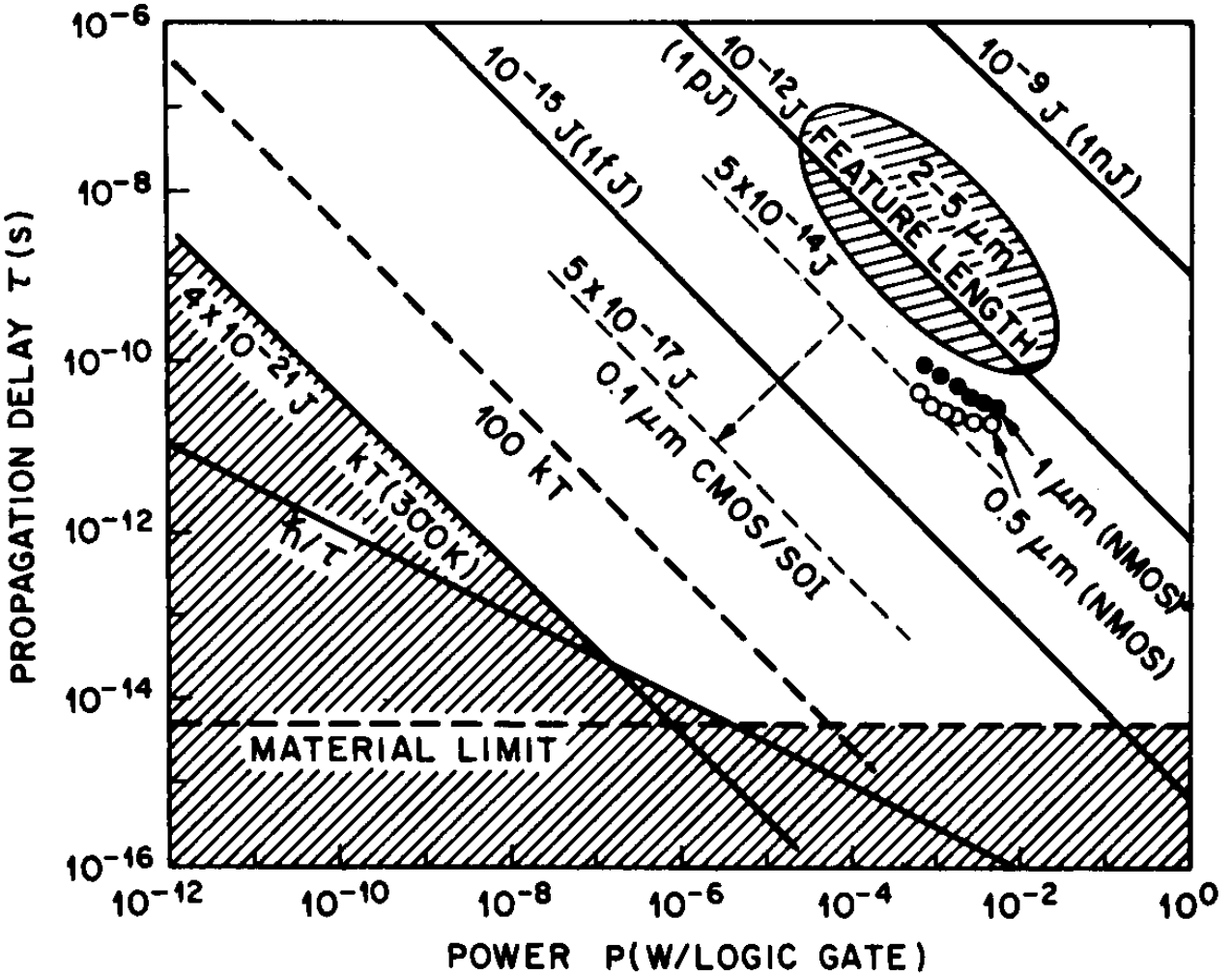
$$P_D = fCV_{DD}^2$$



Delay-power product定義為

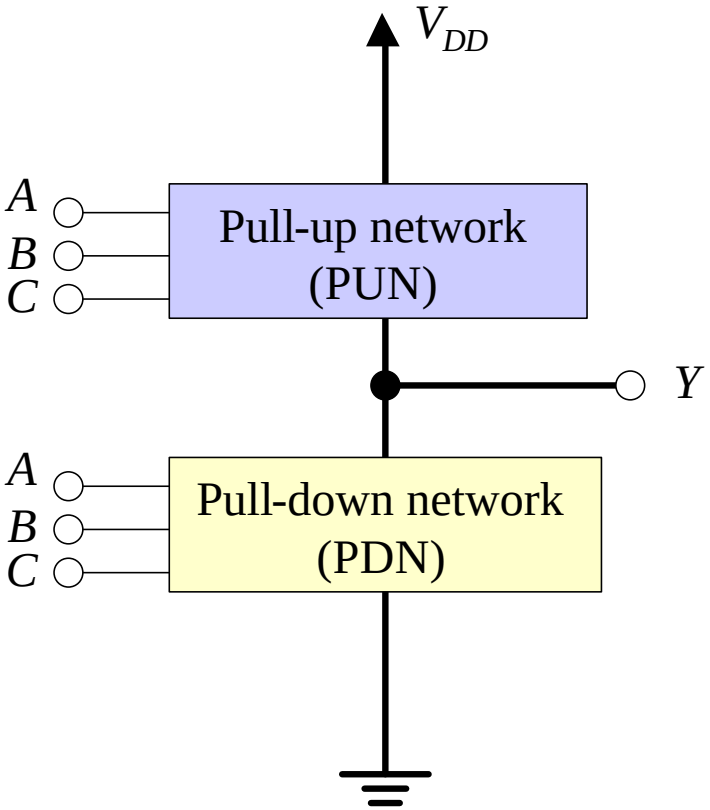
$$DP = P_D t_P$$

對CMOS $DP = CV_{DD}^2$


PROPAGATION DELAY τ (S)
POWER P(W/LOGIC GATE)
10^-6
10^-8
10^-10
10^-12
10^-14
10^-16
10^-12
10^-10
10^-8
10^-6
10^-4
10^-2
10^0
10^-15 J (1fJ)
10^-12 J (1pJ)
10^-9 J (1nJ)
5x10^-14 J
5x10^-17 J
0.1 μm CMOS/SOI
100 kT
4x10^-21 J
kT(300K)
k/τ
MATERIAL LIMIT
2-5 μm FEATURE LENGTH
1 μm (NMOS)
0.5 μm (NMOS)

常見的CMOS邏輯閘

一般結構



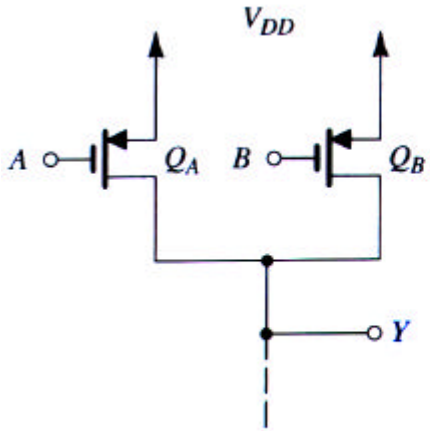
若要使輸出Y為高(1)，須要求PUN各併聯電路至少有一導通（串聯電路全導通），且PDN各併聯電路無一導通（串聯電路至少有一不導通）。

若要使輸出Y為低(0)，須要求PFN各併聯電路至少有一導通（串聯電路全導通），且PUN各併聯電路無一導通（串聯電路至少有一不導通）。

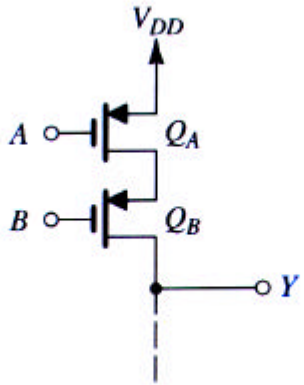
PUN由PMOS構成
PDN由NMOS構成

PUN和PDN必須配合設計

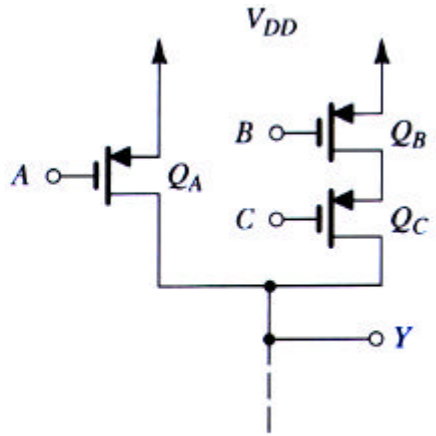
一些PUN電路設計



$Y = \overline{A} + \overline{B}$

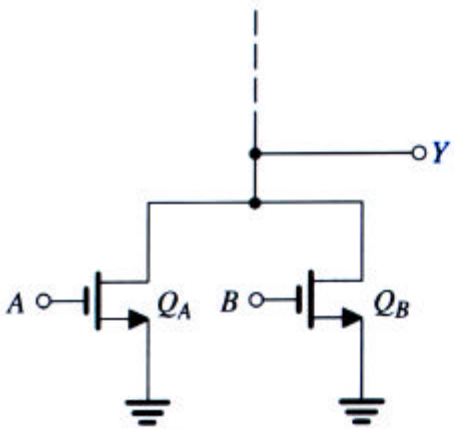


$Y = \overline{A}\,\overline{B}$

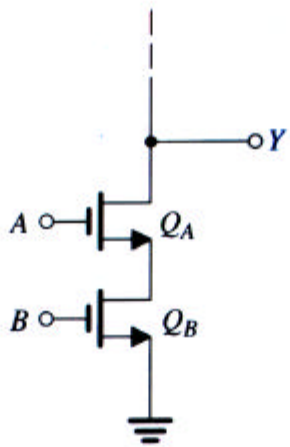


$Y = \overline{A} + \overline{B}\overline{C}$

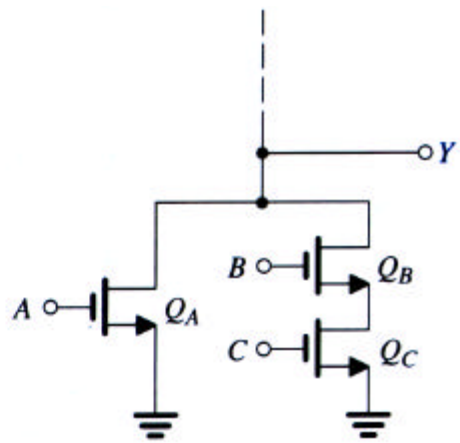
一些PDN電路設計



$\overline{Y} = A + B$

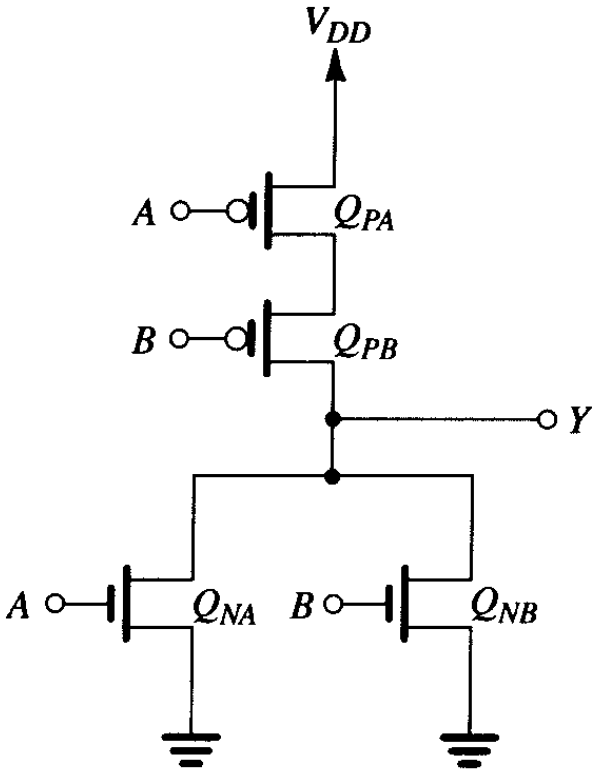


$\overline{Y} = AB$



$\overline{Y} = A + BC$

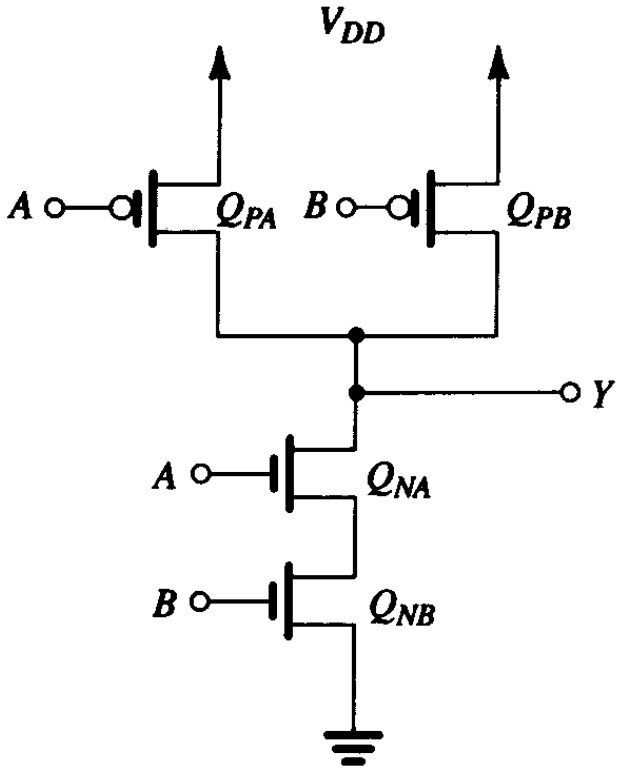
A two-input CMOS NOR gate



$$Y = \overline{A + B}$$

$$\overline{Y} = A + B$$

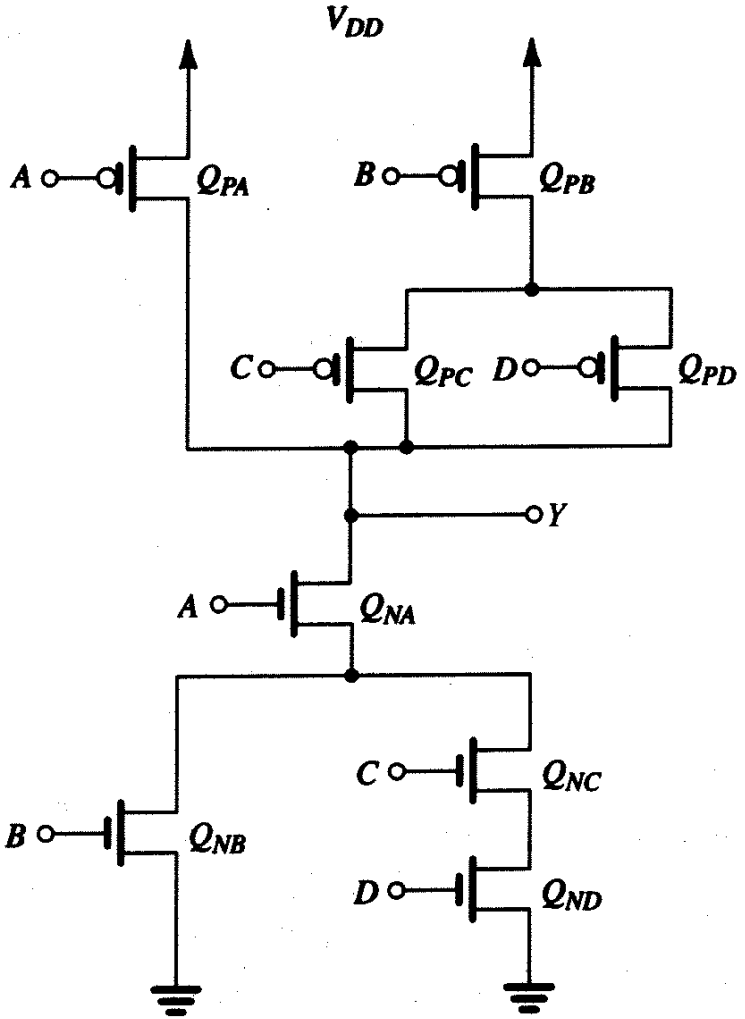
A two-input CMOS NAND gate



$$Y = \overline{AB}$$

$$\overline{Y} = AB$$

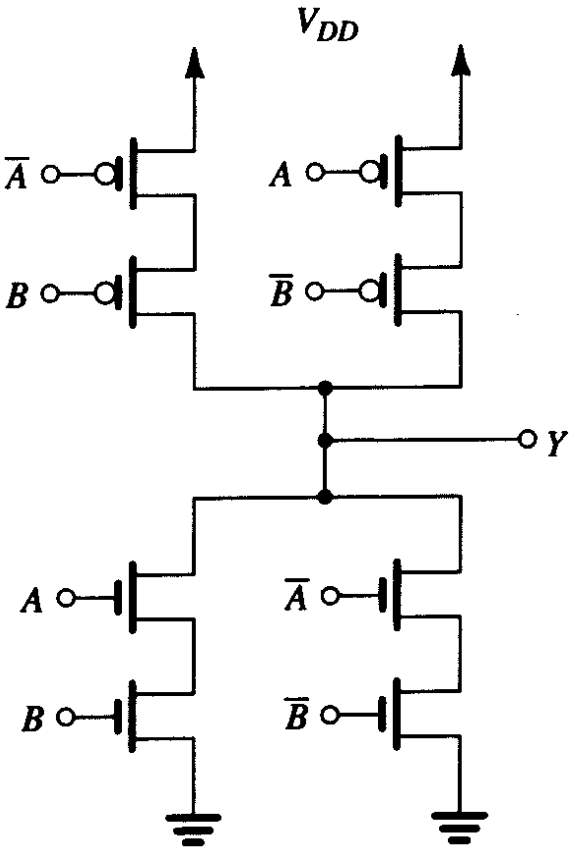
一個稍微複雜的電路



$$Y = \overline{A(B + CD)}$$

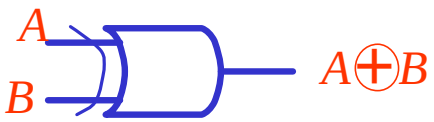
$$\overline{Y} = A(B + CD)$$

Exclusive-OR Function



$$Y = A\overline{B} + \overline{A}B$$

$$\overline{Y} = AB + \overline{A}\,\overline{B}$$

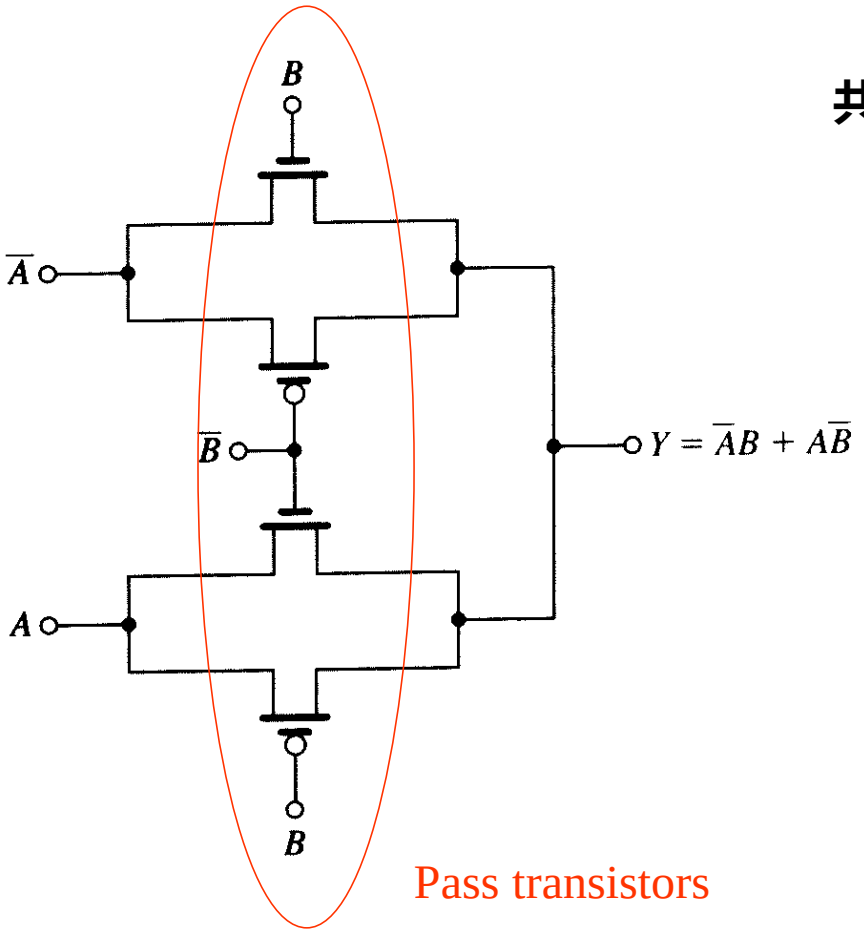


A	$\overline{A}$	B	$\overline{B}$	Y	$\overline{Y}$
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	1	1	0
1	0	1	0	0	1

1位元不含進位的加法器
共需12個MOSFETs

MOSFET個數少的Exclusive-OR function

將MOSFET用作開關

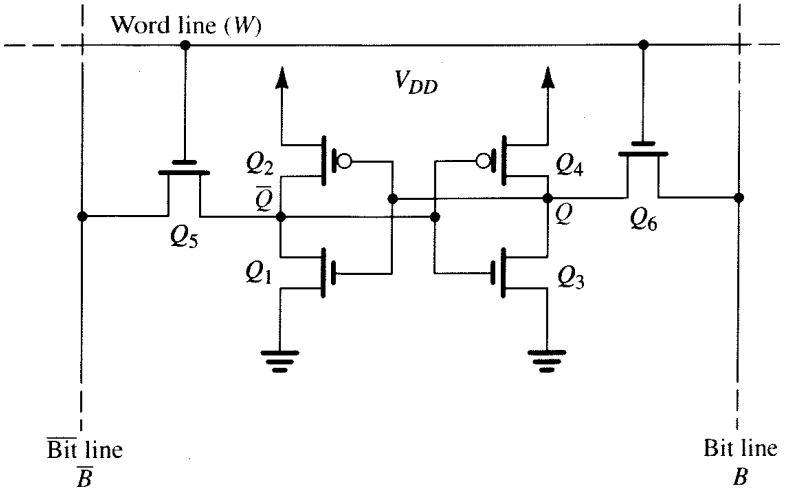


共用8個MOSFETs

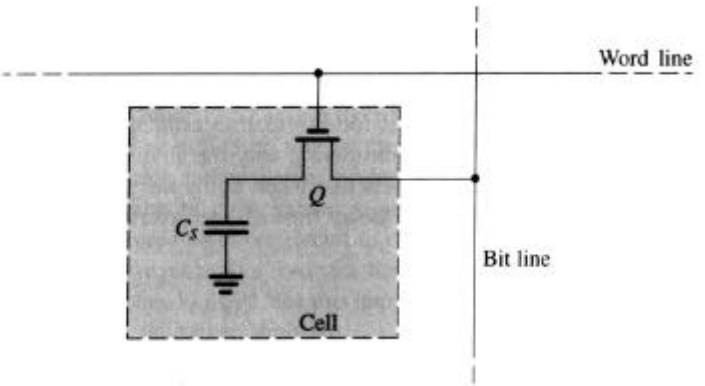
Pass transistors

Static Random-Access Memory (SRAM)

and Dynamic Random-Access Memory (DRAM)



A SRAM cell



A DRAM cell